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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/616,414

07/08/2003

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2110-78-3

9298

7590

09/02/2004

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EXAMINER

HO, HOAI V

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/616,414

Applicant(s)

PASCUCCI, LUIGI

Examiner

Hoai V. Ho

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/8/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) was considered.

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.
2. Claims 1-37 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-15, 21-35 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Taito et al. U. S. Patent (USP) No. 5852583.

As per claims 1-3, 12-14, 21-24, 27-33 and 37, Figure 1 of Taito is directed to a line selector for a matrix of memory elements (col. 3, lines 6-10), comprising a plurality of matrix line group selection circuits (WD00-WD03 and WD10-WD13), each one allowing the selection (WLS0-WLS1) of a respective group of lines (WL00-WL13) according to a first address (01- 02 or RAU0-RAU1), each line group including at least one matrix line (WL00), characterized by comprising flag means (L0) associated with each line group, that can be set (WLS0, col. 3, lines 53-56 and col. 4, lines 5-9) to declare a pending status of a prescribed operation to be conducted on the respective line group, and means (TG0) for entrusting the flag means with the selection of the respective line group during the execution of the prescribed operation, in alternative to the respective line group selection circuit, the flag means enabling, when set, the execution of the prescribed operation on the respective line group (col. 3, line 54-64).

As per claims 4 and 5, Taito, starting at col. 4, lines 5-10, discloses the flag means are reset after the respective word line group has been erased.

As per claims 6, 15, 25, 26, 34 and 35, Figure 1 of Taito discloses further comprising setting means (TN01 and TP01) and resetting means (TN02 and TP02), associated with each flag means for setting and, respectively, resetting the associated flag means, the setting means and resetting means being enabled by the respective line group selection circuit according to the first address (col. 3, lines 5-14).

As per claim 7, Figure 1 of Taito discloses lag means comprises a set-reset flip-flop (L00).

As per claim 8, Figure 1 of Taito discloses the means for entrusting the flag means with the selection of the respective line group during the execution of the prescribed operation comprise means (TG0) for disconnecting the line group selection circuit from a respective line group selection signal line, and means (D0) for transferring onto the line group selection signal line a state corresponding to that of the respective flag means.

As per claim 9, Figure 1 of Taito discloses comprising a plurality of word line selection circuits (PSC0), each one associated with a respective line group selection circuit for allowing the selection of at least one word line within a respective group of word lines, according to a second address (00 or RAL0), the word line selection circuits comprising word line driver circuits (D0) for driving potentials of the word lines.

As per claims 10 and 11, Figure 1 of Taito discloses a word line driver reset circuit (TN 15) is associated with each line group selection circuit, activatable (RSTVNN) for resetting the word line driver circuits of the associated word line selection circuit.

Art Unit: 2818

5. Claims 16-20, 22, 23, 27-33, 36 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al. U. S. Patent No. 6222779 (IDS)

As per claims 22, 23, 27-33 and 37, Figure 18 of Saito a line selection circuit for selecting a group of lines of an array of memory cells (111), the circuit comprising: a selection circuit (112 and 113) operable to select a group of memory cells from the array for an operation; and a status circuit (116) coupled to the selection circuit and operable to enable the selection circuit to perform the operation on a subset of the group of selected memory cells (col. 19, lines 66 and 67).

As per claims 16-20 and 36, Figure 22 of Taito discloses further comprising applying at least one erase pulse.

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Bautista, Jr. et al. (USP 6331951) and Korsh et al. (USP 5901089) discloses a method of erase verification. Roscher et al. (USP 5923609) and Chishiki (USP 5361237) disclose a word line reset circuit.

7. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Art Unit: 2818

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1777. Other inquiries of this application should be called to (571) 272-1562 or the fax number (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



H. Ho
August 7, 2004



Hoai V. Ho
Primary Examiner
Art Unit 2818